

Amendments to the Claims:

Please cancel claims 1-6 and add new claims 7-16 as follows:

1.-6. (Canceled)

7. (New) A semiconductor device of IGBT comprising:

a top region of a second conductivity type;

a deep region of the second conductivity type;

an intermediate region of a first conductivity type for isolating the top region and the deep region;

a collector region of the first conductivity type contacting with the deep region and being isolated from the intermediate region by the deep region;

an emitter electrode connected with the top region;

a collector electrode connected with the collector region; and

a trench gate facing a portion of the intermediate region via an insulating layer, wherein the portion facing the trench gate isolates the top region and the deep region, and wherein the trench gate extends along a longitudinal direction and width of the trench gate varies along the longitudinal direction.

8. (New) A semiconductor device according to claim 7,

wherein a plurality of trench gates extending in parallel is provided, and variations of width of trench gates along the longitudinal direction are aligned in phase between adjacent trench gates.

9. (New) A semiconductor device according to claim 7,

wherein a side wall of the trench gate at a wider width is parallel with a side wall of an adjacent trench gate.

10. (New) A semiconductor device according to claim 9,

wherein variations of width of each trench gate along the longitudinal direction are repeated cyclically along the longitudinal direction.

11. (New) A semiconductor device according to claim 10,

wherein a pair comprising a wide trench gate and a narrow trench gate is repeated along the longitudinal direction, and total length of the wide trench gates is 30 to 80 % of the total length of the trench gate.

12. (New) A semiconductor device according to claim 11,
wherein a plurality of trench gates extending in parallel is provided, and variations of width of trench gates along the longitudinal direction are aligned in phase between adjacent trench gates.

13. (New) A semiconductor device according to claim 12,
wherein width of the intermediate region interposed between adjacent wide trench gates is narrow such that the intermediate region interposed between adjacent wide trench gates becomes a depressed region when on-voltage is not being applied to the trench gates, and the top region is located above the intermediate region interposed between adjacent wide trench gates.

14. (New) A semiconductor device according to claim 7,
wherein variations of width of each trench gate along the longitudinal direction are repeated cyclically along the longitudinal direction.

15. (New) A semiconductor device according to claim 14,
wherein a pair comprising a wide trench gate and a narrow trench gate is repeated along the longitudinal direction, and total length of the wide trench gates is 30 to 80 % of the total length of the trench gate.

16. (New) A semiconductor device according to claim 7,
wherein width of the intermediate region interposed between adjacent wide trench gates is narrow such that the intermediate region interposed between adjacent wide trench gates becomes a depressed region when on-voltage is not being applied to the trench gates, and the top region is located above the intermediate region interposed between adjacent wide trench gates.